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(56) Documents cited
 **GB 1233545 A EP 0195607 A2 EP 0187016 A2
 EP 0098652 A2**

(58) Field of search
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(54) **A lateral insulated gate field effect transistor and a method of manufacture**

(57) A transistor has a semiconductor body (1) having a first region (2) of one conductivity type adjacent a surface of the semiconductor body (1), source and drain regions (3 and 4) of the opposite conductivity type are formed spaced-apart within the first region (2) adjacent the given surface, a lowly doped extension region (5) extends beneath an insulating layer (6) on the given surface from the drain region (4) towards the source region (3), an insulated gate (7) is provided on the given surface (1a) for defining a gateable connection of the source and drain regions (3 and 4), and a further region (10) of the opposite conductivity type is provided adjacent the given surface beneath the insulating layer (6) so as to adjoin the lowly doped extension region (5) remote from the drain region (4) to define a conduction channel area (1) between the source (3) and the further region (10) beneath the insulated gate (7) so that the gateable connection of the source and drain regions is provided between the source and further regions (3 and 10). In the manufacture of the transistor, the insulated gate (7) and insulating layer (6) are used as a mask for the introduction of the impurities to form the source, drain and further regions (3, 4 and 10). Two or more further regions may be provided between the source and drain. The invention may be applied to a lateral insulated gate bipolar transistor structure.

Fig.2.
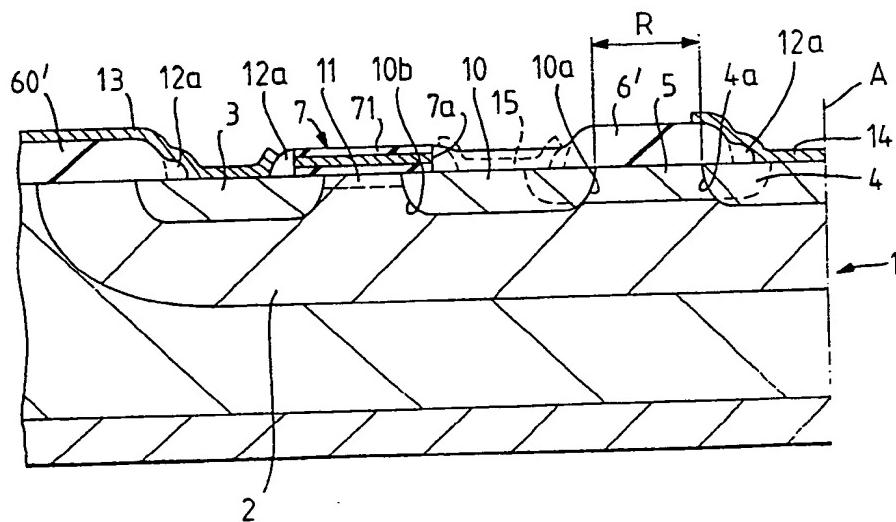
GB 2 215 515 A

Fig.1.
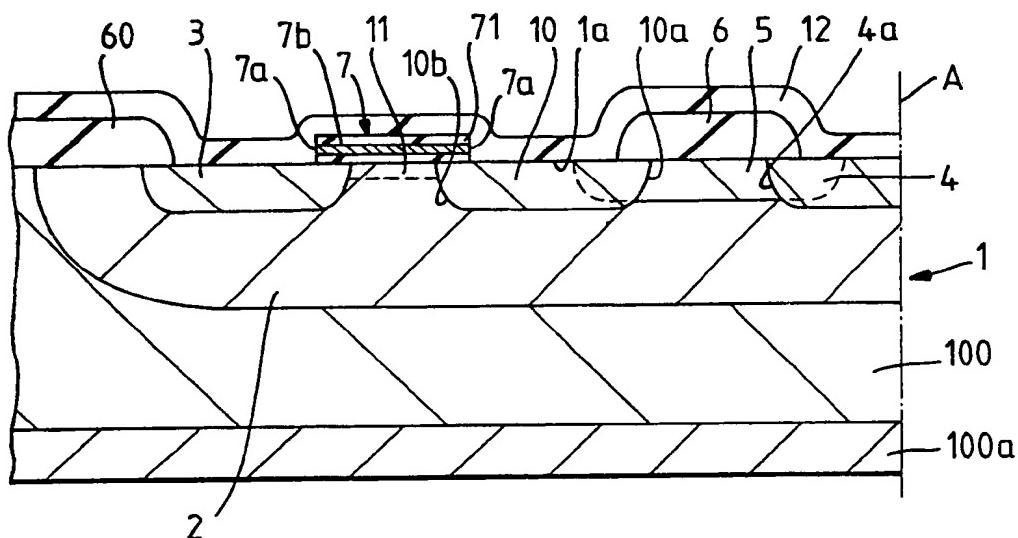
Fig.2.
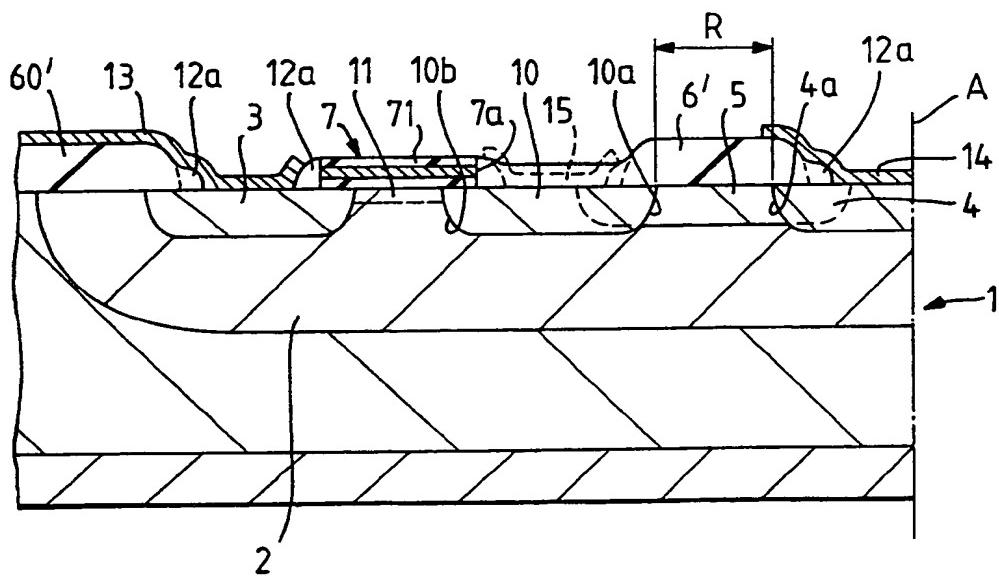
Fig.3.
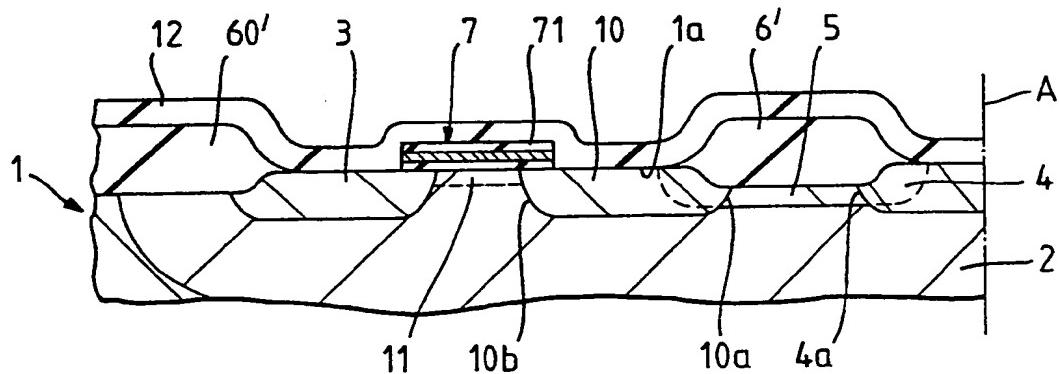
Fig.4.
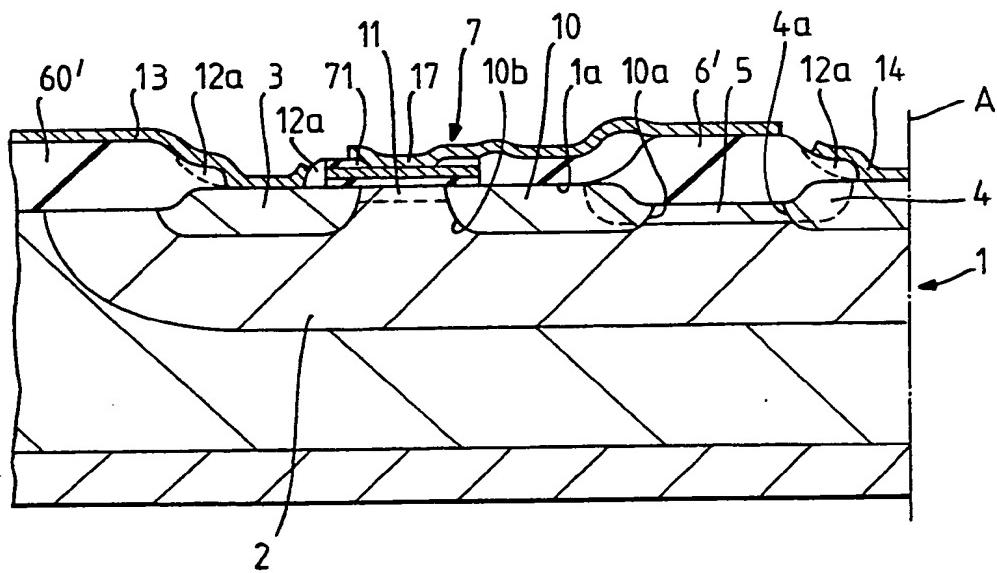
2215515

Fig.5.
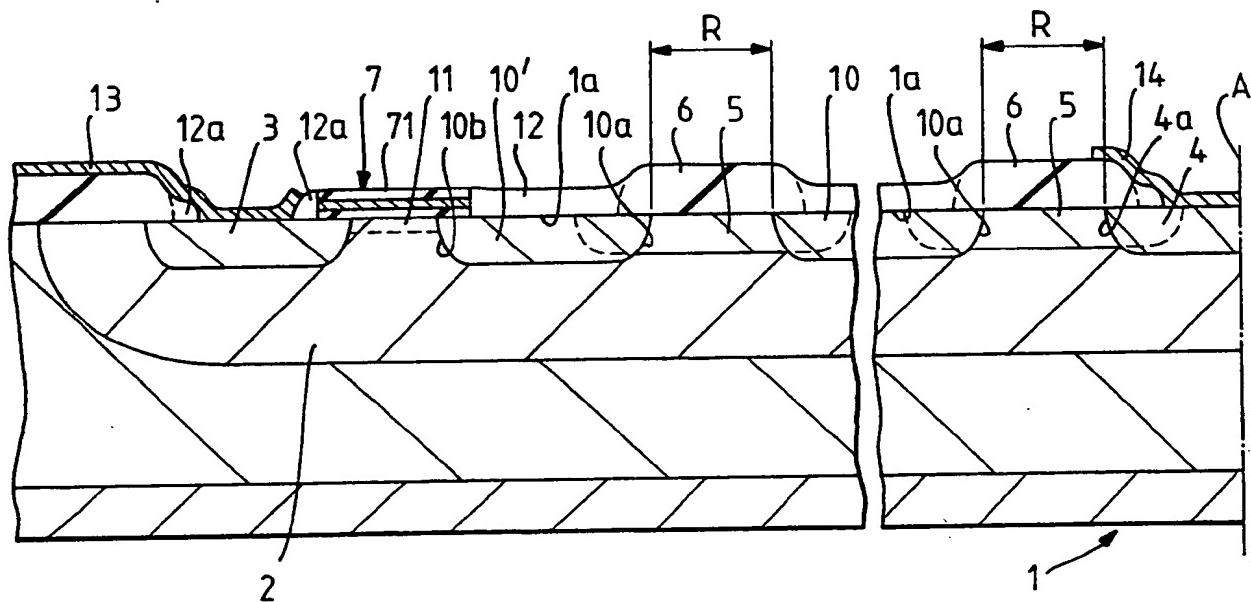
Fig.6.
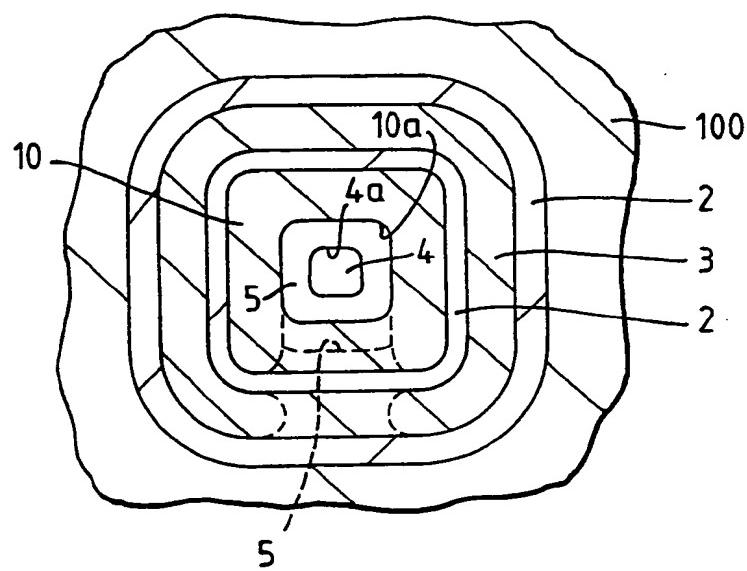
A LATERAL INSULATED GATE FIELD EFFECT TRANSISTOR
AND A METHOD OF MANUFACTURING SUCH A TRANSISTOR

This invention relates to a lateral insulated gate field
effect transistor and a method of manufacturing such a transistor.

Lateral insulated gate field effect transistors are well known
which comprise a semiconductor body having a first region of one
conductivity type adjacent a given surface of the semiconductor
body, source and drain regions of the opposite conductivity type
formed space-apart within the first region and adjacent the given
surface, a lowly doped extension region of the opposite
conductivity type adjoining the drain region and an insulated gate
provided on the given surface for defining a gateable connection of
the source and drain regions.

The provision of such a lowly doped extension region adjoining
the drain region of an insulated gate field effect transistor
enables relatively high source-drain voltages to be applied without
electrical breakdown to lateral insulated gate field effect
transistors where the majority current flow is parallel rather than
perpendicular to the given surface of the semiconductor body. The
use of such lowly doped extension regions is described in many
publications, see for example EP-A-70101 and Siemens Forschungs-und
Entwicklungs Berichte Bd 9(1980) Nr. 4 pages 190 to 194.

Although the inclusion of such a lowly doped extension region
is desirable, the use of such a lowly doped extension region means
that it is no longer easy to use the insulated gate as a mask to
introduce the impurities to form the source and drain regions so
that the source and drain regions are auto-aligned to the insulated
gate and, if a non-auto-aligned method is used, provision has to be
made in the dimensions of the device for mask alignment tolerances.

According to one aspect of the present invention, there is
provided an insulated gate field effect transistor comprising a
semiconductor body having a first region of one conductivity type
adjacent a given surface of the semiconductor body, source and
drain regions of the opposite conductivity type formed spaced-apart

within the first region and adjacent the given surface, a lowly
dop d xtension r gion of th opposite conductivity typ adjoining
the drain region and extending beneath an insulating layer on the
given surface from the drain region towards the source region and
an insulated gate provided on the given surface for defining a
gateable connection of the source and drain regions, characterised
in that a further region of the opposite conductivity type is
provided adjacent the given surface beneath the insulating layer
and adjoining the lowly doped extension region remote from the
drain region to define a conduction channel area between the source
region and the further region beneath the insulated gate so that
the gateable connection of the source and drain regions is provided
between the source and further regions.

According to a second aspect of the present invention there is
provided a method of manufacturing a lateral insulated gate field
effect transistor, which method comprises providing a semiconductor
body having a first region of one conductivity type adjacent a
given surface of the semiconductor body, introducing impurities to
form a lowly doped extension region of the opposite conductivity
type adjacent the given surface within the first region, defining
an insulated gate on the given surface spaced from the lowly doped
extension region, introducing impurities using the insulated gate
as a mask to form source and drain regions of the opposite
conductivity type adjacent the given surface within the first
region with the drain region adjoinging the lowly doped extension
region so that the insulated gate defines a gateable connection of
the source and drain regions, characterised by defining an
insulating layer on the given surface within the periphery of the
lowly doped extension region and spaced from the insulated gate and
introducing the impurities to form the source and drain regions
using the insulated gate and the insulating layer as a mask so as
to form a further region of the opposite conductivity type which
adjoins the lowly doped extension region remote from the drain
region and defines a conduction channel area beneath the insulated
gate between the source region and the further region so that the

gateable connection of the source and drain regions is provided between the source and further regions.

An insulated gate field effect transistor in accordance with the invention may thus be formed in an auto-aligned manner so that the the properties of the insulated gate field effect transistor do not depend upon mask tolerances and are therefore more reproduceable. Furthermore, in use of an insulated gate field effect transistor embodying the invention the voltage at the further region follows the voltage applied to the drain region. Thus at relatively low voltages the drain region is resistively coupled to the further region by the lowly doped extension region, whilst at higher voltages the relatively lowly doped extension region becomes fully depleted of free charge carriers so that drain and further regions are coupled by a depletion region with the voltage difference between the drain and further regions being determined by the separation of the drain and further regions for a given doping and thickness of the lowly doped extension region. Thus, by selecting the separation of the drain and further regions appropriately, which in a method embodying the invention can be done simply by selecting the dimensions along the given surface of the insulating layer, the voltage at the further region can be maintained, for a given maximum expected drain voltage, below that at which breakdown would occur at the pn junction between the further region and the second region. When an appropriate gate voltage is applied to the insulated gate of an insulated gate field effect transistor in accordance with the invention a conduction channel, an inversion channel in the case of an enhancement or normally off transistor, is provided in the conduction channel area between the source and further regions enabling charge carriers to be injected from the source region via the conduction channel into the further region and then to be swept through the depletion region to the drain region.

Embodiments of the invention will now be described, by way of example, with reference to the accompanying drawings, in which;

Figure 1 is a cross-sectional view of part of a semiconductor

body illustrating a stage in a first embodiment of a method in accordance with the invention for manufacturing an insulated gate field effect transistor in accordance with the invention;

Figure 2 is a cross-sectional view similar to Figure 1 illustrating an insulated gate field effect transistor manufactured using the first embodiment of a method in accordance with the invention;

Figure 3 is a cross-sectional view of a portion of part of a semiconductor body illustrating a stage in a second embodiment of a method in accordance with the invention for manufacturing an insulated gate field effect transistor in accordance with the invention;

Figure 4 is a cross-sectional view similar to Figure 1 illustrating an insulated gate field effect transistor manufactured using the second embodiment of a method in accordance with the invention;

Figure 5 is a cross-sectional view of part of a semiconductor body illustrating a further embodiment of an insulated gate field effect transistor in accordance with the invention; and

Figure 6 is a schematic plan view illustrating one possible geometrical arrangement for an insulated gate field effect transistor in accordance with the invention.

It should, of course, be understood that the Figures are merely schematic and are not to scale, various dimensions, especially thickness having been relatively exaggerated or reduced in the interests of clarity.

Referring now to the drawings, there are illustrated various embodiments of insulated gate field effect transistors in accordance with the invention. In each case, the insulated gate effect transistor comprises a semiconductor body 1 having a first region 2 of one conductivity type adjacent a given surface 1a of the semiconductor body 1. Source and drain regions 3 and 4 of the opposite conductivity type are formed spaced-apart within the first region 2 and adjacent the given surface 1a and a lowly doped extension region 5 of the opposite conductivity type adjoins the

drain region 4 and extends from the drain region 4 towards the
sourc region 3 beneath an insulating layer 6. An insulated gate 7
provided on the given surface 1a defines a gateable connection
of the source and drain regions 3 and 4 of the insulated gate field
effect transistor. In acordance with the invention, a further
region 10 of the one conductivity type provided adjacent the given
surface 1a beneath the insulating layer 6 adjoins the lowly doped
extension region 5 remote from the drain region 4 to define a
conduction channel area 11 between the source and further regions 3
and 10 beneath the insulated gate 7 so that the gateable connection
of the source and drain regions 3 and 4 is provided between the
source and further regions 3 and 10.

A first embodiment of an insulated gate field effect device in
accordance with the invention will now be described in greater
detail with reference to Figures 1 and 2 in which the dashed line A
indicates a central axis of symmetry.

Referring first to Figure 1, the semiconductor body 1
comprises a lowly doped n-type monocrystalline silicon region 100
which may be an epitaxial layer having a dopant concentration of
about 7×10^{15} atoms cm^{-3} provided on a highly doped
monocrystalline silicon substrate 100a.

After cleaning to remove surface contaminants and to grow a
protective layer of a thermal silicon oxide, p-type impurities, for
example boron, are locally implanted and/or diffused into the
semiconductor body 1 via the given surface 1a using an appropriate
mask to provide the first region 2 as a p-type well having, for
example, a dopant concentration adjacent the surface of about
1.5×10^{16} atoms cm^{-3}.

Again using conventional masking techniques, n-type impurities
are locally introduced into the semiconductor body via the given
surface 1a so as to form the lowly doped extension region 5 within
the p well or first region 2. The dose used to form the lowly doped
extension region 5 is sufficiently low that the lowly doped
extension region 5 forms a RESURF (REduced SUrface Field) region
which, as described in detail, for example in a paper entitled

'High voltage thin layer devices (RESURF devices)' by J.A. Appel et
al published in Philips Journal of Research, Vol. 35 No. 1 1980 at
pages 1-13, is a region which is sufficiently thin and sufficiently
lowly doped so that, under reverse-bias, the region becomes fully
depleted of free charge carriers thereby spreading the field lines
laterally so as to reduce the surface field, prior to the reverse
breakdown voltage of the pn junction being reached. As indicated
in the aforementioned paper in order to function as a RESURF
region, the product Nd of the thickness (or depth) d in cm and the
doping concentration N in atoms cm^{-3} of the region should be
of the order of 2×10^{12} atoms cm^{-2}. Typically, the lowly doped
extension region may have a dopant concentration adjacent the
surface of about 2×10^{16} atoms cm^{-3}.

After formation of the lowly doped extension region 5, silicon
dioxide is thermally grown on the given surface 1a to form a
relatively thick, for example, 1000 Angstroms, field oxide layer.
The field oxide layer is then patterned or defined using
conventional photolithographic and etching techniques to provide a
layer of field oxide 60 surrounding the periphery of the area in
which the insulated gate field effect transistor is being formed
and also to provide the insulating layer 6 which overlies a central
portion of the lowly doped extension region 5. A relatively thin
layer of gate oxide is then grown by a conventional thermal process
on the given surface 1a. Polycrystalline silicon is then deposited
onto the gate oxide layer and appropriately doped, usually using
phosphorus, to provide the necessary conductivity. A covering
insulating layer, for example of silicon oxide or silicon nitride,
is deposited onto the doped polycrystalline silicon layer.
Alternatively of course, an oxide layer may be grown by thermal
oxidation of part of the polycrystalline silicon. The gate oxide
layer, doped polycrystalline silicon layer and covering insulating
layer are patterned or defined using conventional photolithographic
and etching techniques to define the insulated gate 7 and a
protective insulating layer cover 71 for the insulated gate 7.

It should, of course, be appreciated that other conductive

materials could be used for the conductive gate layer, for example a metal could be used instead of the doped polycrystalline silicon.

After deposition of a protective scatter oxide, n-type impurities, for example arsenic or phosphorus, are introduced into the semiconductor body 1 via the given surface 1a using the insulated gate 7 and field oxide 60, 6 as a mask so as to form the source and drain regions 3 and 4 and the further region 10. By this process, the source region 3 and the further region 10 are both auto-aligned to the insulated gate 7 so that the length of the conduction channel area 11 is defined by the lateral diffusion beneath the insulated gate 7 of the dopants introduced to form the source and further regions 3 and 10. The inner periphery 10a of the further region 10 and the periphery 4a of the drain region 4 are auto-aligned to the insulating layer 6 and are arranged to overlap the lowly doped extension 5. The extent of the lowly doped region 5 between the inner periphery 10a of the further region 10 and the periphery 4a of the drain region 4 is thus defined by the extent in that direction of the insulating layer 6. The source, drain and further regions 3, 4 and 10 may have, for example, a dopant concentration adjacent the surface of about 1×10^{20} atoms cm^{-3}.

After conventional cleaning of the surface, a further layer of insulating material 12 is deposited by a conventional chemical deposition technique to cover the entire surface.

Windows may then be opened using conventional masking and photolithographic techniques to enable metallisation to contact the source and drain regions 3 and 4 and to provide connection to the insulated gate 7. Alternatively, as indicated in Figure 2, an anisotropic etching technique, for example a plasma etching technique, may be used to etch back the insulating material layer 12 using the silicon oxide or silicon nitride insulating layer cover 71 as an etch stop so that the conductive surface 7b of the insulated gate 7 is not exposed by the anisotropic etching. In this example, the area over the further region 10 is masked during the anisotropic etching so that the further region 10 remains covered by the insulating material layer 12. Such an anisotropic etching

technique leaves fillets r spacers 12a of insulating material on
side walls 7a of the insulated gate 7 and on side walls 60a, 6a of
the field oxide pattern. Metallisation, for example aluminium, may
be deposited and patterned to define contacts 13 and 14 to the
source and drain regions, respectively, with the spacers 12a on the
side walls 7a of the insulated gate 7 serving to isolate the
insulated gate 7 from the metallisation 13, 14.

     As shown in Figure 2, the source metallisation 13 may extend
up onto the field oxide 60 and the drain metallisation 14 may
similarly extend up onto the insulating layer 6 so as to provide a
field plating effect.

     In use of the insulated gate field effect transistor shown in
Figure 2, when the voltages applied to the source and drain
metallisations 13 and 14 are very small, the lowly doped extension
region 5 provides a resistive connection between the drain region 4
and the further region 10. At higher operational voltages, the
lowly doped extension region 5 becomes fully depleted of free
charge carriers and the depletion region of the drain region 4
extends to the further region 10 so that the further region 10 is
coupled to the drain region 4 by the depletion region. The voltage
at the further region 10 will thus follow the voltage at the drain
region 4 and will be at a voltage lower than the voltage applied to
the drain region 4, the difference in voltage being determined by
the separation R by the lowly doped extension region 5 of the drain
region 4 and the further region 10 and also by the doping and
thickness of the lowly doped extenion region 5 which will determine
when the lowly doped extension region 5 becomes fully depleted so
that the depletion region couples the further region 10 to the
drain region 4. Thus, by selecting the separation of the drain and
further regions 4 and 10 by selecting the dimensions along the
given surface 1a of the insulating layer 6, the insulated gate
field effect transistor can be designed so that, for a given
maximum expected drain voltage, the voltage drop along the
depletion region to the further region 10 is sufficient that the
reverse-biassing voltage across the pn junction 10b between the

first region or well 2 and the further region 10 is below the
breakdown voltage of the pn junction 10b. When an appropriate gate
voltage is applied to the insulated gate 7, an inversion channel is
induced in the conduction channel area 11 between the source region
3 and the further region 10 enabling charge carriers, in this
example electrons, to be injected from the source region 4 via the
inversion channel 11 into the further region 10 from whence the
charge carriers are swept through the depletion region coupling the
further region 10 and the drain region 4 to the drain region 4.
Thus a conductive path is provided between the source region 3 and
the drain region 4 via the gateable connection between the source
and further regions 3 and 10 and via the depletion region which
extends through the lowly doped extension region 5 to couple the
drain and further regions 4 and 10.

Figures 3 and 4 illustrate a modified version of the insulated
gate field effect transistor.

As will be appreciated from a comparison of Figures 2 and 4,
the insulated gate field effect transistor is very similar to that
shown in Figure 2 with the exception that the field oxide pattern
is formed using a local oxidation of silicon (LOCOS) technique. The
area of the insulating material layer 12 over the further region 10
is again masked during the anisotropic etching step.

In view of the similarities with the arrangement described
with respect to Figures 1 and 2, the arrangement of Figures 3 and 4
will only be briefly described with reference to those areas where
the method used differs.

Thus, after introduction of the impurities to form the p-well
or first region 2, a silicon nitride mask is deposited and defined
on the given surface 1a. With the area at the periphery of the
region in which the insulated gate effect transistor is being
defined masked by a subsequent photoresist mask, the n-type
impurities are introduced to form the lowly doped extension region
5. The photoresist mask is then removed and a thermal oxidation
process carried out as is known in the art so that the given
surface 1a of the semiconductor body is locally oxidised in those

areas not protected by the silicon nitride mask so as to define the peripheral field oxide 60' and the insulating layer 6'. The lowly doped extension region 5 is thus self-aligned to the insulating layer 6.

After removal of the silicon nitride mask, the method proceeds as described above with reference to Figures 1 and 2. Thus, after deposition of the insulating material layer 12, the surface of the insulating material layer 12 overlying the further region 10 is masked so that the anisotropic etching does not expose the surface of the further region 10. The metallisation can then be patterned and defined to form the source and drain metallisation 13 and 14 as before. Also if a window is opened in the insulating layer 7a using appropriate conventional masking and photolithographic techniques prior to depositing the metallisation a field plate 17 may be provided extending from the insulated gate 7 over the remaining portion of the insulating material layer 12a and the insulating layer 6 towards the drain region 4.

The insulated gate field effect transistor shown in Figure 4 operates in a manner similar to that described in Figures 1 and 2, the method used to manufacture the insulated gate field effect transistor shown in Figure 4 having the advantage that the lowly doped extension region 5 is auto-aligned to the subsequently formed insulating layer 6 by use of the LOCOS technique.

Figure 5 illustrates yet a further insulated gate field effect transistor in accordance with the invention. As shown in Figure 5, the insulated gate field effect transistor is similar in structure to that shown in Figure 2, but has two or more further regions 10 connected together via the lowly doped extension region 5 so as to provide a conductive path from the innermost further region 10a to the drain region 4. As will be appreciated from the above, the number of further regions 10 provided is defined merely by the appropriate patterning of the insulating layer 6.

The provision of two (or more) further regins 10 enables, as will be appreciated by those skilled in the art of providing floating ring edge termination systems for semiconductor devices

(see for example EP-A-182422), a larger voltage drop from the drain region to the inner(most) further region than can be obtained with a single further region. Thus, by providing additional further regions higher voltages can be catered for whilst still enabling the voltage at the inner(most) further region 10 to be below the breakdown voltage. It may also be possible to vary the dimensions and/or separations of the further regions 10, for example to vary the width and separation as in E-A-182422 with the widest further region being adjacent the drain region 4.

Otherwise, the transistor shown in Figure 5 is manufactured in the same way as the transistor shown in Figure 2. Of course, two or more further regions can be provided in the transistor structure shown in Figure 4 by appropriately redefining the silicon nitride mask used for the LOCOS oxidation.

An insulated gate field effect transistor in accordance with the invention may have any desired geometry when viewed in plan, that is when viewed perpendicular to the given surface 1a. Figure 6 illustrates schematically the given surface 1a of a device in accordance with the invention with surface features such as insulating layers 6, 60, insulated gate 7 and metallisation omitted in interests of clarity. Thus, as can be seen from Figure 6, the device has a square (with rounded corners) geometry with all the regions being concentric about the central drain region 4. Although the lowly doped extension region 5 is shown as a solid annular region, it may be possible by appropriate redefinition of the insulating layer 6 to define the lowly doped extension region as discrete areas interconnecting the drain region 4 and the further region(s) 10.

Although in the arrangements described above and shown in the Figures, the insulating material overlying the further region(s) 10 is masked during the anisotropic etching step, this need not necessarily be the case. Thus, as indicated in phantom lines in Figure 2, the anisotropic etching may be allowed to expose the surface of the further region 10 and during patterning of the metal deposited to form the source, gate and drain metallisation a metal

contact 15 (again shown in phantom lines in Figure 2) may be
provided n the further region(s) 10 although no electrical
connection would be made to the contact 15.

It should, of course, be appreciated that where the concentric
geometry shown in Figure 6 is adopted, it may be necessary to
provide breaks in the surrounding metallisation to enable contact
to the drain region 4. In such circumstances the necessary breaks
may be provided by masking a strip of the insulating layer 12 prior
to the etching step so that after the surfaces of the source and
drain regions 3 and 4 (and possibly also the further region 10)
have been exposed, a strip of insulating material radiates
outwardly from the drain region over the further region 10, the
insulate gate 7 and the source region 3 providing a path along
which the drain metallisation may extend insulated from the source
and gate metallisation (and contact 15, if provided). Also, as
indicated by the phantom lines in Figure 6, the source region 3,
insulated gate 7 and further region 10 need not be formed as
complete annuli but could have aligned gaps covered by insulating
material providing a path for the drain metallisation. Such an
arrangement has the advantage that the field oxide pattern can be
used to define the extent of the source region, insulated gate and
further region(s) by appropriate modification of the field oxide
mask and no masking of the insulating layer 12 prior to anisotropic
etching is then required.

In addition, although in the arrangements described above and
shown in the Figures, the insulated gate structure 7 is protected
by an insulating layer cover 71, such an insulating cover need not
necessarily be provided where it is not necessary for
metallisation, for example drain metallisation, to extend over the
insulated gate 7. Thus, the anisotropic etching may be allowed, by
omitting the insulating layer cover 71, to expose the surface 7b of
the conductive gate layer, that is the doped polycrystalline
silicon layer in the examples given above. Such exposure of the
insulated gate surface 7b may be possible for example where the
field oxide pattern is defined or the insulating layer 12 masked

during the subsequent etching so that an insulating material strip
xtends over the source, insulated gate and further regions to
provide a path for the drain metallisation insulated from the
source, insulated gate and further regions or, for example, where a
linear geometry is used, that is with the source, insulated gate
and drain arranged in a line, so that there is no need for
metallisation to cross over underlying regions or gates.

Once the surface areas of the source and drain regions 3 and 4
(possibly also the surface of the insulated gate and/or of the
further region 10) have been exposed, a self-aligned silicide
process may be used so as to enable better contact to the
subsequent metallisation. Thus, a layer of titanium may be sputter
deposited onto the surface and then annealed in a nitrogen
containing atmosphere. This process results in the formation of a
silicide layer over the exposed silicon areas but because of the
competing reaction with the nitrogen ambient in a titanium nitride
layer on the silicon oxide surfaces. The titanium nitride area may
then be selectively removed using a known process, leaving a
silicide layer on each of the exposed silicon surface areas.
Metallisation may then be deposited as described above.

To take a particular example, with the arrangement illustrated
in Figure 1 and 2 and a surface geometry similar to that shown in
Figure 6, using the surface dopant concentrations given as examples
in the aforegoing description, an insulated gate field effect
transistor capable of withstanding a source-drain voltage of 50
volts may be obtained by, for example, defining the lowly doped
extension region 5 as an annulus (square with rounded corners)
using a mask window having a width (along the surface 1a) of about
5.5 micrometres with a central opening of a width of about
1 micrometre. Of course, the lowly doped extension region 5 need
not necessarily be annular but could be a solid region without a
central aperture.

In such an example, the field oxide is defined so as to
provide the insulating layer 6 as an annulus concentric with and
lying wholly within the lowly doped extension region so as to have

a width f ab ut 3.5 microm tr s and the insulated gate 7 is defined s as to similarly be f annular shape with a width of about 2 micrometres and spaced apart two micrometres from the insulating layer 6 so that two micrometre wide windows are provided

5 through which the impurities are introduced to form the source, drain and further regions 3, 4 and 10 which may be of about the same thickness or depth as the lowly doped extension region 5 and is typically in the range of about 0.2 micrometres to about 0.3 micrometres. The reverse voltage withstanding capabilities may be

10 adjusted simply by altering the width of the insulating layer 6 whilst keeping all other dimensions and dopings constant. Thus, if for a given doping and depth of the lowly doped extension region 5 the width of the insulating layer 6 was reduced, then the reverse-voltage between the source and drain regions 3 and 4 which

15 could be reached before breakdown would be reduced whereas if the width of the insulating layer 6 was increased, then the reverse-voltage between the source and drain regions 3 and 4 which could be reached before breakdown, would be increased. To take an example with the above given dimensions and dopings, then a

20 reduction in the width of the insulating layer 6 to 3.0 micrometres would reduce the maximum reverse biassing voltage which could be withstood from 50 volts to 46 volts.

Although in the arrangement shown in Figure 6, the insulated gate field effect transistor is symmetric about the axis A through

25 the drain region 4, the transistor could, if desired, be symmetric about the source region 3 or a linear arrangement could be used. Such alternative arrangements may however require additional edge termination arrangements such as field plates and/or floating or Kao's ring systems to ensure that breakdown does not occur at the

30 exposed drain region. The invention may be applied to a lateral insulated gate bipolar transistor structure, that is where a p-type region is provided adjacent the given surface adjoining the drain region 4 so as to provide conductivity modulation of the conduction channel areas. Also by appropriate doping of the channel area 11,

35 the insulated gate field effect transistor may be a normally on

(depletion) rather than a normally off (enhancement) mode device.
Of course, the conductivity types given in the examples d scribed
above may be reversed. Furthermore, an insulated gate field effect
transistor in accordance with the invention may be integrated into
the semiconductor body with other devices. Thus, for example, one
or more insulated gate field effect transistors in accordance with
the invention may be formed in the same semiconductor body as a
power device such as a vertical power MOSFET with the p-well or
second region 2 providing the necessary junction isolation.

From reading the present disclosure, other modifications will
be apparent to persons skilled in the semiconductor art for example
persons skilled in the design, manufacture and/or use of
semiconductor devices. Although claims have been formulated in
this application to particular combinations of features, it should
be understood that the scope of the disclosure of the present
application also includes any novel feature or novel combination of
features disclosed herein either explicitly or implicitly or any
generalisation or modification of that feature or of one or more of
those features whether or not it relates to the same invention as
presently claimed in any claim. The applicants hereby give notice
that new claims to such features and/or combinations of such
features may be formulated during the prosecution of the present
application or of any further application derived therefrom.

CLAIMS

1. A lat ral insulated gate field eff ct transistor comprising
a semiconductor body having a first region of one conductivity type
adjacent a given surface of the semiconductor body, source and
5   drain regions of the opposite conductivity type formed spaced-apart
within the first region and adjacent the given surface, a lowly
doped extension region of the opposite conductivity type adjoining
the drain region and extending beneath an insulating layer on the
given surface from the drain region towards the source region and
10   an insulated gate provided on the given surface for defining a
gateable connection of the source and drain regions, characterised
in that a further region of the opposite conductivity type is
provided adjacent the given surface beneath the insulating layer
and adjoining the lowly doped extension region remote from the
15   drain region to define a conduction channel area between the source
region and the further region beneath the insulated gate so that
the gateable connection of the source and drain regions is provided
between the source and further regions.

2. A transistor according to Claim 1, wherein two or more
20   further regions are provided between the source and drain regions
and are connected by the lowly doped extension region so that the
conduction channel area is defined beneath the insulated gate
between the source region and one further region and the gateable
connection of the source and drain regions is provided between the
25   source region and the said one further region.

3. A transistor according to Claim 1 or 2, wherein a field
plate extends from the insulated gate over the insulating layer
towards the drain region.

4. An insulated gate field effect transistor substantially as
30   hereinbefore described with reference to and/or as illustrated in
the accompanying drawings.

5. A method of manufacturing a lateral insulated gate field
effect transistor, which method comprises providing a semiconductor
body having a first region of one conductivity type adjacent a
35   given surface of the semiconductor body, introducing impurities to

form a lowly doped extension region of the opposite conductivity
type adjacent the giv n surface within the first region, d fining
an insulated gate on the given surface spaced from the lowly doped
extension region, introducing impurities using the insulated gate
as a mask to form source and drain regions of the opposite
conductivity type adjacent the given surface within the first
region with the drain region adjoining the lowly doped extension
region so that the insulated gate defines a gateable connection of
the source and drain regions, characterised by defining an
insulating layer on the given surface within the periphery of the
lowly doped extension region and spaced from the insulated gate and
introducing the impurities to form the source and drain regions
using the insulated gate and the insulating layer as a mask so as
to form a further region of the opposite conductivity type which
adjoins the lowly doped extension region remote from the drain
region and defines a conduction channel area beneath the insulated
gate between the source region and the further region so that the
gateable connection of the source and drain regions is provided
between the source and further regions.

6. A method according to Claim 5, which comprises defining the
insulating layer so as to provide one or more apertures in the
insulating layer overlying the lowly doped extension region and
introducing the impurities to form the source, drain and further
regions of the opposite conductivity type using the insulated gate
and the insulating layer as a mask so that two or more further
regions connected by the lowly doped extension region are provided
between the source and drain regions, with the source region and
further region closest to the source region being aligned to
opposite edges of the insulated gate.

7. A method according to Claim 5 or 6, which method comprises
providing a field plate extending over the insulating layer from
the insulated gate towards the drain region.

8. A method according to Claim 5, 6 or 7, which comprises
forming the insulating layer by local oxidation of the given
surface of th semiconductor body.

9. A method f manufacturing an insulated gate field effect transistor substantially as hereinbefore described with reference to th accompanying drawings.

10. Any novel feature or combination of features described herein.

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